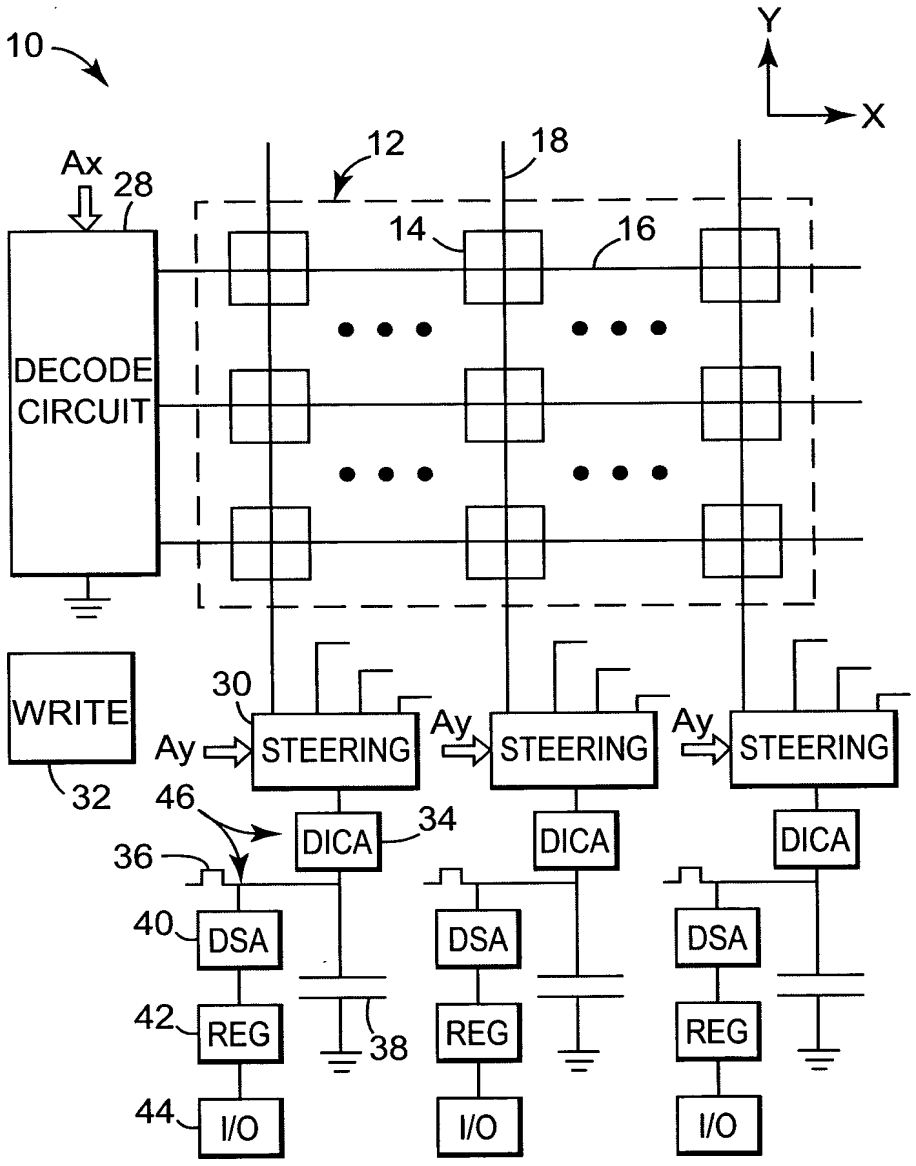
10
Y
X
12
18
Ax
28
14
16
DECODE CIRCUIT
WRITE
32
30
Ay
STEERING
Ay
STEERING
Ay
STEERING
46
DICA
34
DICA
DICA
36
40
DSA
DSA
DSA
42
REG
38
REG
REG
44
I/O
I/O
I/O

Fig. 1

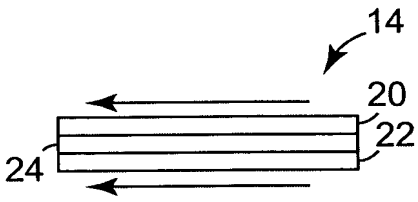

Fig. 2A

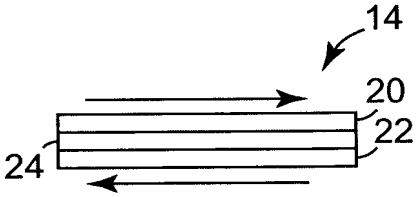

Fig. 2B

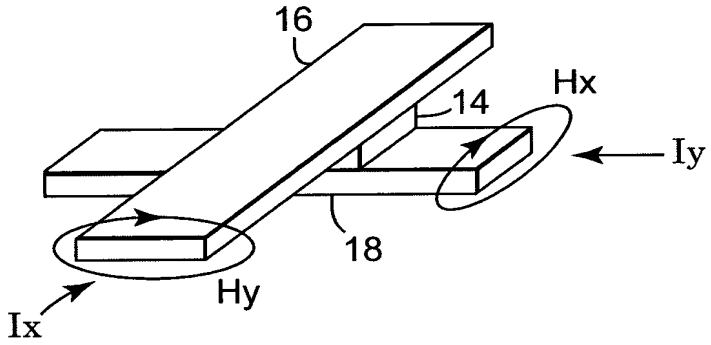

Fig. 3

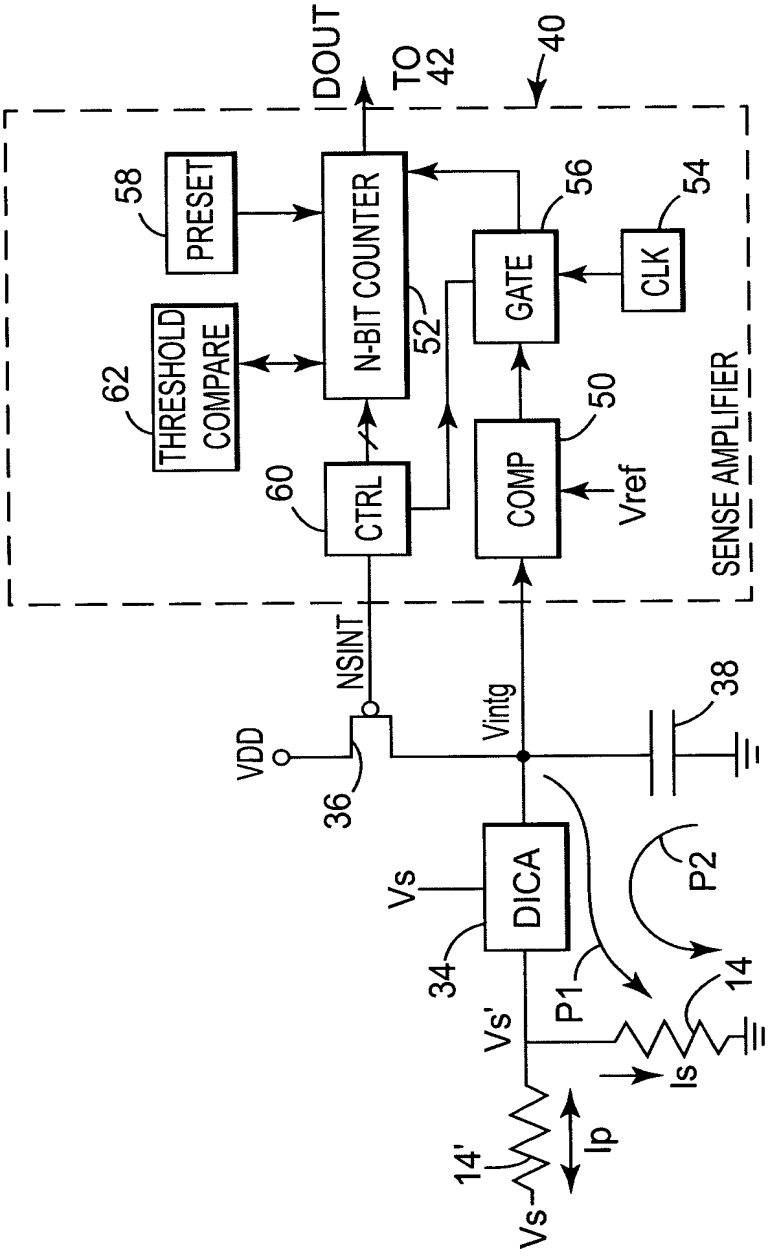
DOUT
TO 42
40
58
PRESET
N-BIT COUNTER
52
56
GATE
54
CLK
62
THRESHOLD COMPARE
60
CTRL
COMP
50
Vref
SENSE AMPLIFIER
NSINT
Vintg
38
VDD
36
Vs
DICA
34
P2
P1
14
Vs'
Is
14'
Ip
Vs

Fig. 4

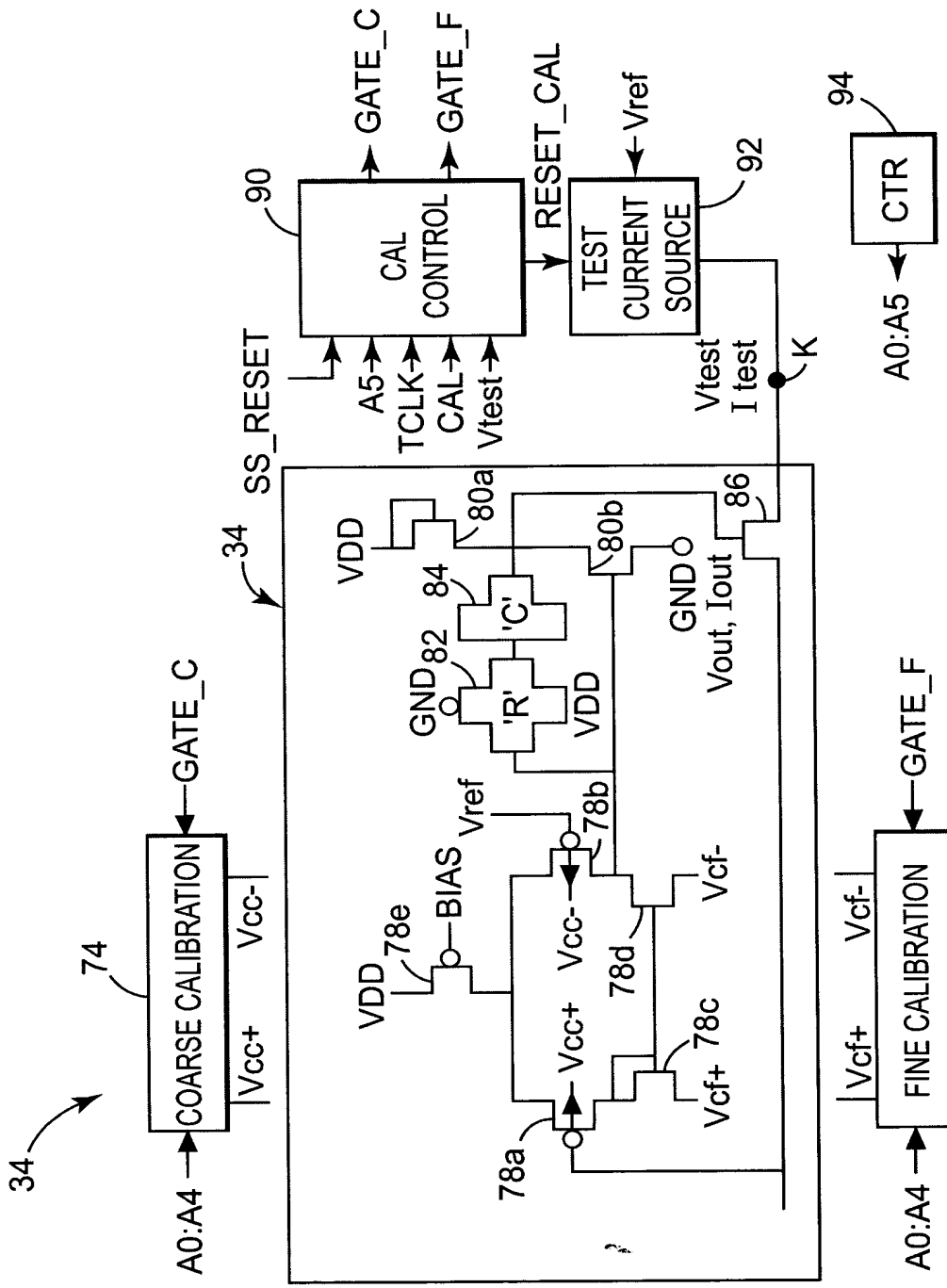
GATE_C
GATE_F
RESET_CAL
Vref
94
90
CAL CONTROL
TEST CURRENT SOURCE
92
CTR
A0:A5
SS_RESET
A5
TCLK
CAL
Vtest
Vtest
I test
K
34
80a
80b
86
VDD
84
'C'
GND
82
'R'
VDD
GND
Vout, Iout
Vref
78b
BIAS
78e
VDD
Vcc-
Vcc+
78d
Vcf-
78c
Vcf+
78a
74
COARSE CALIBRATION
Vcc-
Vcc+
GATE_C
A0:A4
34
Vcf-
Vcf+
FINE CALIBRATION
76
GATE_F
A0:A4

Fig. 5

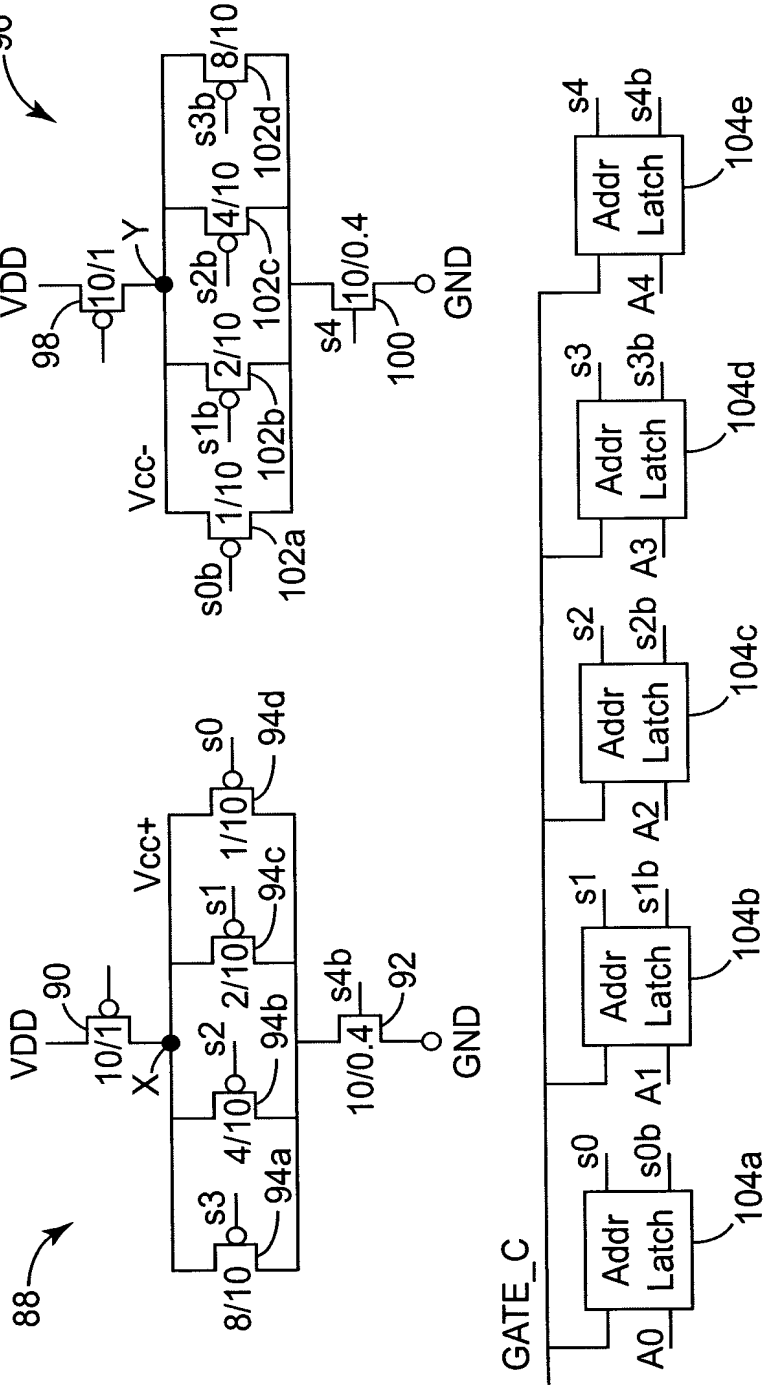
96
VDD
98
10/1
Y
Vcc-
s0b
1/10
102a
s1b
2/10
102b
s2b
4/10
102c
s3b
8/10
102d
s4
10/0.4
100
GND
88
VDD
90
10/1
X
Vcc+
8/10
s3
4/10
94a
s2
2/10
94b
s1
1/10
94c
s0
94d
s4b
10/0.4
92
GND
GATE_C
Addr Latch
A0
s0
s0b
104a
A1
s1
s1b
104b
A2
s2
s2b
104c
A3
s3
s3b
104d
A4
s4
s4b
104e
74

Fig. 6

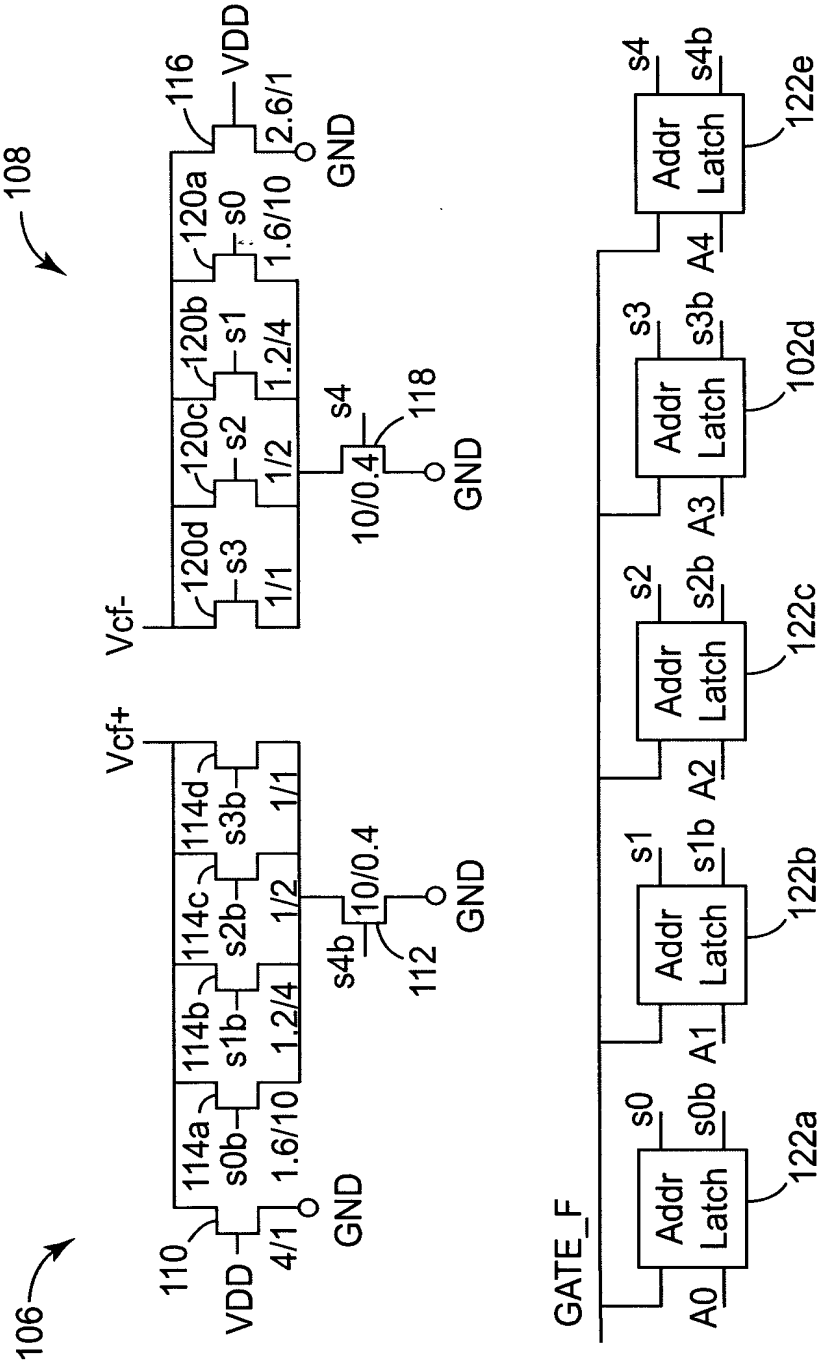
106
108
110
VDD
4/1
GND
114a
s0b
1.6/10
114b
s1b
1.2/4
114c
s2b
1/2
114d
s3b
1/1
Vcf+
s4b
10/0.4
112
GND
Vcf-
120d
s3
1/1
120c
s2
1/2
120b
s1
1.2/4
120a
s0
1.6/10
116
VDD
2.6/1
GND
s4
10/0.4
118
GND
GATE_F
A0
Addr
Latch
s0
s0b
122a
A1
Addr
Latch
s1
s1b
122b
A2
Addr
Latch
s2
s2b
122c
A3
Addr
Latch
s3
s3b
102d
A4
Addr
Latch
s4
s4b
122e
76

Fig. 7

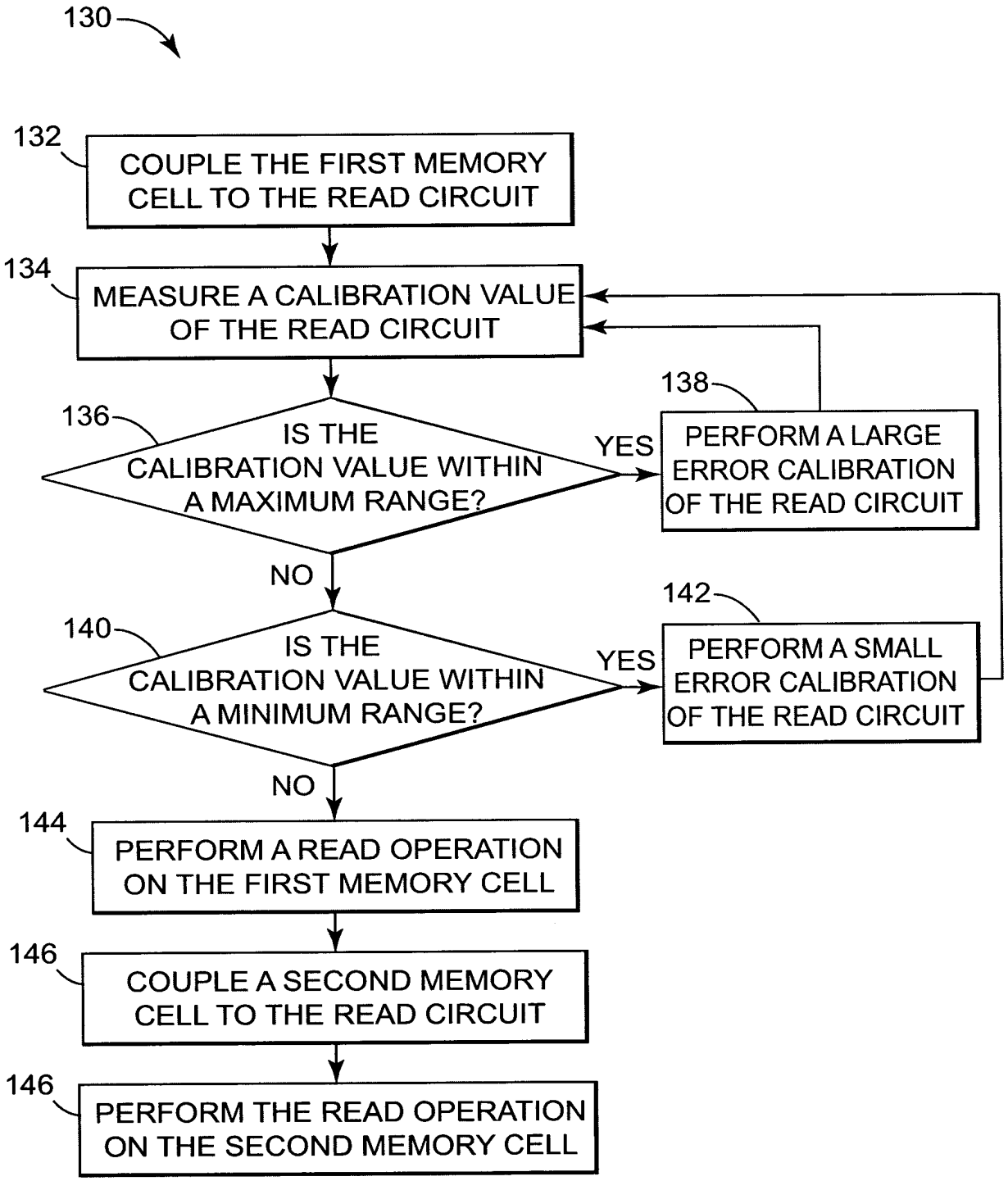
130
132
COUPLE THE FIRST MEMORY CELL TO THE READ CIRCUIT
134
MEASURE A CALIBRATION VALUE OF THE READ CIRCUIT
136
IS THE CALIBRATION VALUE WITHIN A MAXIMUM RANGE?
YES
138
PERFORM A LARGE ERROR CALIBRATION OF THE READ CIRCUIT
NO
140
IS THE CALIBRATION VALUE WITHIN A MINIMUM RANGE?
YES
142
PERFORM A SMALL ERROR CALIBRATION OF THE READ CIRCUIT
NO
144
PERFORM A READ OPERATION ON THE FIRST MEMORY CELL
146
COUPLE A SECOND MEMORY CELL TO THE READ CIRCUIT
146
PERFORM THE READ OPERATION ON THE SECOND MEMORY CELL

Fig. 8